IT IS CLAIMED:

1. A method of programming data into a reprogrammable non-volatile memory system of a type having blocks of memory cells that are simultaneously erasable and which individually store a given number of host units of data, comprising responding to host programming commands by programming data in one of two designated blocks depending at least in part upon a number of host units of data specified by the host programming commands that have sequential logical addresses.

2. A method of writing data into a non-volatile memory system of a type having blocks of memory cells that are simultaneously erasable and which individually store a given number of host units of data, comprising:

responding to host commands to write units of data having non-sequential logical addresses by writing the data with sequential physical addresses into a first designated block, and

responding to host commands to write units of data having sequential logical addresses equal to or in excess of a given proportion of said given number by writing the data into a second designated block.

3. The method of claim 2, wherein writing data to the first designated block includes writing a number of host units of data into the first designated block having sequential logical addresses less than said given number.

4. The method of claim 2, wherein the non-volatile memory cells are organized into multiple sub-arrays and said blocks of memory cells include memory cells of two or more of the sub-arrays.

5. In a non-volatile memory having memory cells organized in a plurality of groups of one or more blocks of a minimum number of cells that are simultaneously erasable and storing a given number of pages of data at specified page numbers, a method of updating data in less than the given number of pages of a first programmed group of blocks, comprising:

designating at least first and second blocks to receive updated data of less than the given number of pages of the first programmed group of blocks,

writing data of one or more pages having a number of sequential logical addresses less than a predetermined number to pages of the first designated block, and

writing data of a plurality of pages with a number of sequential logical addresses equal to or in excess of the predetermined number of pages to the second designated block.

6. The method of claim 5, including updating data in less than the given number of pages of a second programmed group of blocks, comprising:

writing data of one or more pages having a number of sequential logical addresses less that said predetermined number to pages of the first block.

7. The method of claim 5 wherein, in response to a level of updating less than the predetermined number of pages in the first programmed group of blocks, the first designated block is dedicated to receive updated data for only the first programmed group of blocks.

8. In a non-volatile memory having memory cells organized in groups of one or more blocks of a minimum number of cells that are simultaneously erasable and wherein a given number of pages of data are programmed into individual ones of the groups of blocks, a method of updating data in less than all pages of a given group of one or more blocks, comprising:

determining whether at least one predefined condition of the data update is satisfied, and

if it is determined that the condition is satisfied, thereafter writing the updated pages of data into pages of a first other group of one or more blocks having page numbers selected independently of the page numbers of the pages of data within the given group of blocks that are being updated, or

if it is determined that the condition is not satisfied, thereafter writing the updated pages of data into correspondingly numbered pages of a second other group of one or more blocks.

9. The method of claim 8, wherein, if the condition is not satisfied, data from pages of the given group of blocks not being updated is combined into a common one of the groups of blocks in correspondingly numbered pages with the updated data in other pages of the common group of blocks.

10. The method of claim 8, wherein the condition includes the number of pages being updated being less than a predetermined proportion of said given number of pages in the given group of blocks.

11. The method of claim 8, wherein the first other group of blocks is utilized to store updated versions of pages of a plurality of the individual groups of blocks including said given block.

12. The method of claim 8, wherein the first other block is utilized to store updated versions of pages of only said given group of blocks.

13. The method of claim 8, which additionally comprises consolidating data by copying both pages from the given group of blocks that have not been updated and pages from the first other group of blocks that are updated versions of data pages of the given group of blocks into a previously erased group of blocks in page number locations that correspond to those of the given group of blocks.

14. The method of claim 13, wherein the data consolidating is caused to occur repetitively at intervals after a plurality of occurrences of updating data in less than all pages of the given group of blocks.

15. The method of claim 13, which additionally comprises, after consolidating data, erasing data from said first another block.

16. The method of claim 8, additionally comprising designating said first other group of blocks to store updated versions of pages of only said given group of blocks in response to the existence of at least one data writing pattern being noted.

17. The method of claim 16, wherein said at least one data writing pattern includes repetitive writing operations to one or more pages of said given group of blocks.

18. The method of claim 16, wherein said at least one data writing pattern includes repetitively writing one or a few pages of data during individual writing operations that are less than written during a majority of the writing operations.

19. The method of claim 16, wherein said at least one data writing pattern includes designating the given group of blocks to store overhead data of others of the plurality of groups of blocks.

20. In a non-volatile memory having memory cells organized in groups of one or more blocks of a minimum number of cells that are simultaneously erasable and wherein a given number of host units of data are programmed into individual ones of the groups of one or more blocks, a method of updating less than all the data stored in a given group of one or more blocks in response to a host command, comprising:

designating at least a first group of one or more blocks to store in sequential physical block locations host units of data within a first range of logical addresses without regard to whether the logical addresses of such data are sequential or not, and

designating at least a second group of one or more blocks to store host units of data within a second range of logical addresses with sequential logical addresses therein designated for sequential physical locations with an address offset of zero or more.

21. The method of claim 20, wherein the first group of blocks may contain an update of data contained within the second group of blocks with a common logical address.

22. The method of claim 20, wherein the first group of blocks may contain data having a logical address that is not represented by data in the second group of blocks.

23. The method of claim 20, wherein the first and second ranges of logical addresses contain common addresses of logical blocks.

24. The method of claim 20, wherein the first and second ranges of logical addresses contain no common addresses of logical blocks.

25. A memory system, comprising:

an array of non-volatile memory cells organized into a plurality of sub-arrays that individually include addressing, programming and reading circuits, the sub-arrays being divided into units of memory cells that are erased together, the erase units further being divided into units of cells that are programmed together, the programming units being identified by programming unit offset addresses within their erase units,

a controller that controls operation of the memory cell array,

at least one erase unit within individual ones of the sub-arrays being designated by the controller to store updated data of sequentially addressed programming units of a first group of one or more others of the erase units within individual ones of the sub-arrays in programming units having the same address order as the programming units within said at least one other of the erase units and with an address offset of zero or more, and

at least another erase unit within individual ones of the sub-arrays being designated by the controller to store updated data of programming units of a second group of one or more others of the erase units within individual ones of the sub-arrays in pages according to a predetermined sequence without regard to the address sequence or programming unit offset of the programming unit data being updated.